EPCglobal™ Generation 2 RFID

MONZA/ID

Features

- Unique ID factory-programmed and permalocked into special 64-bit memory field for enhanced anti-counterfeiting/anti-cloning capability.
- Compliant to:
  - EPCglobal™ UHF Gen 2
  - ISO/IEC 18000-6C, and
  - ISO/IEC 15963 (UID standard)
- Dual antenna input maximizes range and provides for orientation indifference.
- High receptivity yields eight-meter read range, six-meter write range, and excellent tag sensitivity—even when buried deep within a pallet of RF-absorbing material.
- Extended temperature range (–40 °C to +65 °C) for reliable performance under harsh conditions.
- Patented interference rejection affords robust performance in noisy environments.
- Impinj's field-rewritable NVM (optimized for RFID) with 96-bit EPC provides programming flexibility and 100,000-cycle/50-year retention reliability.
- Available preprogramming of customer EPCs at the wafer level delivers a fast, reliable, and cost-effective turnkey manufacturing solution.
- A key component of the Impinj GrandPrix™ Solution, Monza™ tag silicon is *RFID that just works*™.

Overview

An essential component of Impinj's GrandPrix™ solution, Monza/ID tag silicon delivers the many features empowered by the UHF Gen 2 standard, including superior tag throughput and compliance with global spectral regulations. The EPCglobal Gen 2 specification is the ultimate standard for automatic identification requirements ranging from items to cases to pallets, worldwide. For inventory control, unique item tracking, logistics, product integrity, security, and data accuracy, the use of Monza/ID-powered tags yields unprecedented supply chain visibility and confidence.

The 64 bits of unique, serialized ID memory are factory programmed and permenatly locked, providing a robust solution for tagging applications that require authentication measures beyond the 96-bit EPC.

In addition, Monza/ID establishes new benchmarks for range, readability, and high-speed field rewriteability. And in keeping with Impinj's ground-breaking quality standards, Monza/ID chips are 100% factory tested. Furthermore, Monza/ID's nonvolatile memory (NVM) features 100,000 cycle/50-year retention reliability.

Monza/ID tag silicon also benefits from Impinj's innovative Self-Adaptive Silicon® core technology, which enables the creation of a true RFID system-on-a-chip integrating leading-edge analog, digital, and memory functions on a single die no larger than a grain of sand. It's a significant Impinj advantage that yields major performance, sourcing, and cost improvements over competing products. More importantly, the Impinj family of RFID products represents the best performing tag silicon available, exhibiting outstanding receptivity, as well as ESD protection characteristics that are critical for ensuring inlay manufacturability at the highest assembly speeds.

Finally, Monza/ID is supported by a growing family of innovative antenna designs that not only optimize tag performance for wide-ranging requirements and specific market applications, but enable whole new categories of use.

RFID that just works™. *Everywhere.*

Table of Contents

1 Introduction

1.1 Scope

This datasheet defines the physical and logical specifications for Gen 2-certified Monza/ID tag silicon, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2 Reference Documents

EPCglobal™ Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen 2 Specification)
Note: This specification includes normative references, terms and definitions, symbols, abbreviated terms, and notation, the conventions of which were adopted in the drafting of this document.

Impinj Wafer Assembly Specification

Impinj Wafer Map Orientation

EPC™ Tag Data Specification

2 Functional Description

Described are the key functional blocks of the Monza/ID tag silicon, as well as an overview of its operation within a typical application.

2.1 Monza/ID Block Diagram

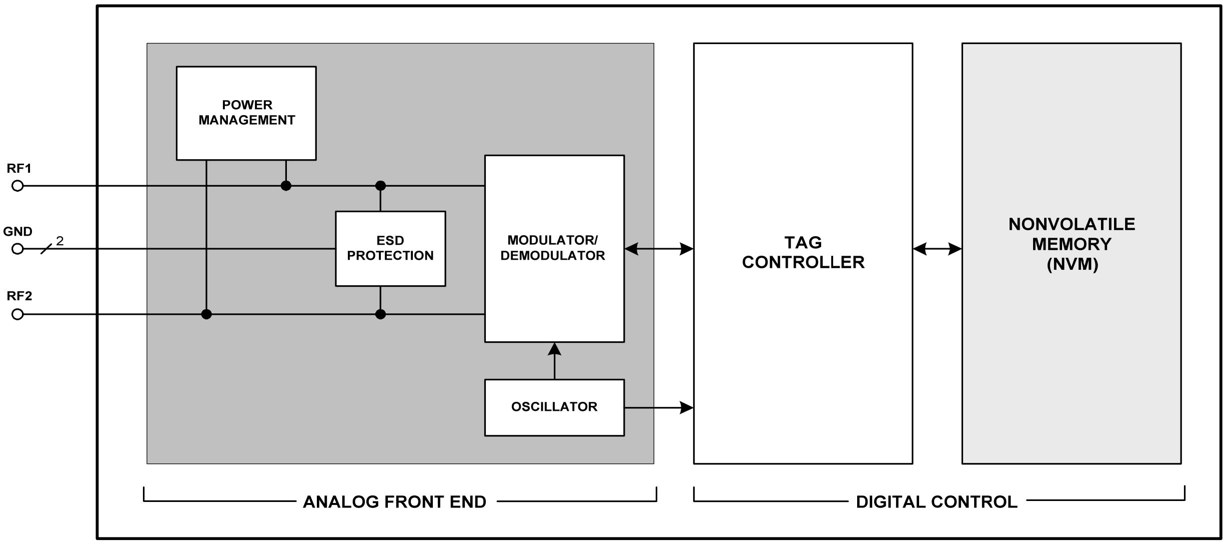


Figure 2-1 Block Diagram

2.2 Pad Descriptions

Monza/ID tag silicon has four external pads available to the user: two antenna pads and two ground pads (the antenna ports are isolated while the ground pads are internally strapped together), as shown in Table 2-1 (see also Figure 2-2).

Table 2-1 Pad Descriptions

External Signals	External Pad	Description
RF1	1	Antenna Input 1
RF2	1	Antenna Input 2
GND	1	Ground
GND	1	Ground

2.3 Dual Antenna Input

All interaction with Monza/ID tag silicon, including generation of its internal power, air interface, negotiation sequences, and command execution, occurs via its two antenna ports and associated grounds.

The dual antenna inputs enable antenna diversity, which in turn minimizes a tag's orientation sensitivity, particularly when the two antennae are of different types (e.g., a combination of loop and dipole) or are otherwise oriented on different axis (X-Y). The dual antenna configuration also enables increased read and write ranges.

The two antenna inputs operate quasi-independently. The power management circuitry receives power from the electromagnetic field induced in the pair, and the demodulator exploits the independent antenna connections, combining the two demodulated antenna signals for processing on-chip.

Monza/ID tag silicon may also be configured to operate using a single antenna port by simply connecting just one of the two inputs. The unused port may be connected to ground (to either, or both ground pads, as they are identical and connected on-chip) or allowed to float. With the exception of the use cases described in section 3.3, the two ports should not be connected to each other, as this will reduce power efficiency.

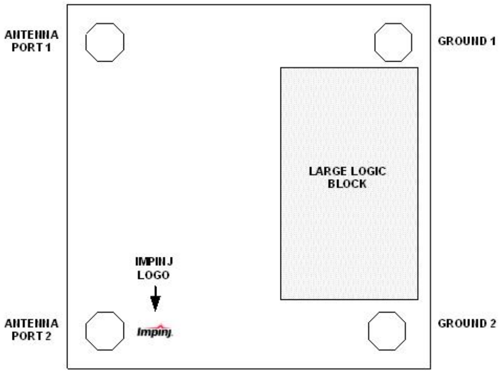


Figure 2-2 Monza/ID Die Orientation

2.4 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader’s RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

2.5 ESD Protection

To divert ESD energy, the ESD Protection block shunts charge from both positive and negative sources when a high voltage is presented across the inputs, thus protecting the chip from damage.

2.6 Modulator/Demodulator

Monza/ID tag silicon demodulates any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna pair between reflective and absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

2.7 Tag Controller

The preceding sections detail the analog functions of power management and signal acquisition and transmission. In the Tag Controller block, we enter the digital domain. While it also performs a number of overhead duties, the heart of this block is the finite state machine logic that carries out the command sequences.

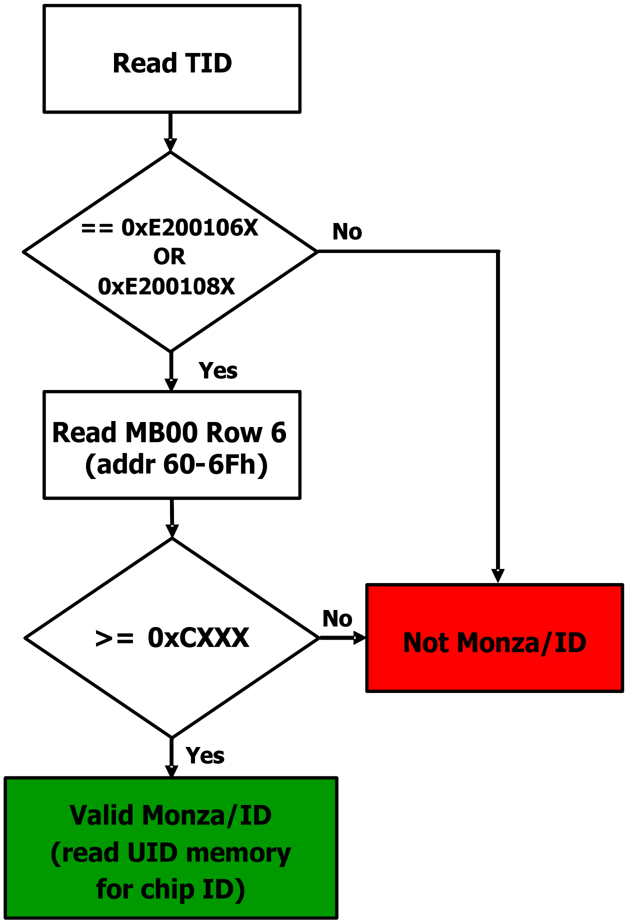
2.8 Nonvolatile Memory

Monza/ID’s embedded memory is based on Impinj’s multiple-times-programmable (MTP), nonvolatile memory (NVM) cell technology, specifically optimized for exceptionally high performance in RFID applications. All programming overhead circuitry is integrated on-chip. Monza/ID NVM provides 100,000 cycle endurance and 50-year data retention.

The NVM block is organized into three segments: 1) EPC memory (96 bits), 2) Reserved memory, and 3) factory-programmed UID memory (the UID occupies the Gen 2 User Memory space). TID memory is ROM-based, and contains Impinj's manufacturer ID (000000000001) and the Monza/ID model number.

2.9 Validating Monza/ID

Authentication using Monza/ID is a three-step process involving serialization, association, and authentication. The simple routine shown in Figure 2-3 will validate that the Monza/ID tag chip is, in fact, authentic and not cloned. The association of the factory-programmed serialized UID (which occupies the Gen 2 User Memory bank) and the item EPC completes the authentication process.



Note: X = Don’t Care.

Figure 2-3 Validating Monza/ID (see Figure 4-1 Physical / Logical Memory Map)

3 Interface Characteristics

Described are the RF interface characteristics of both reader (Forward Link) and tag (Reverse Link).

3.1 Reader-to-Tag (Forward Link) Signal Characteristics

Table 3-1 Forward Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Read Sensitivity Limit		–11.5		dBm	Input sensitivity is measured on a single RF input at 25 °C. Input sensitivity is specified for a R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=6.25μs, PW=2.1μs, and a T=>R link operating at 160kbps with FM0 encoding.
Write Sensitivity Limit		–7			
Maximum RF Field Strength			+20[1]	dBm	
Modulation Characteristics					
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying; phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth (A-B)/A	80		100	%	
Ripple, Peak-to-Peak M_h=M_l			5	%	Portion of A-B
Rise Time ($t_{r,10\text{-}90\%}$)	0		0.33Tari	sec	
Fall Time ($t_{f,10\text{-}90\%}$)	0		0.33Tari	sec	
Tari[2]	6.25		25	μs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX(0.265Tari,2)		0.525Tari	μs	Pulse width defined as the low modulation time (50% amplitude)

Note 1. Reader antenna power with tag sitting on antenna. Assumes tag has half-wave dipole antenna. While maximum radiated reader power is +36 dBm for both Read and Write operations, the maximum power the tag should receive is +20 dBm (see section 5.2).

Note 2. Values are nominal; they do not include reader clock frequency error.

3.2 Tag-to-Reader (Reverse Link) Backscatter

The tag transmits information on the tag-to-reader link by reflecting, or backscattering, part of the incident RF energy from the reader. Backscatter modulation is performed by modulating the input impedance of the tag, thereby modulating the reflection coefficient (denoted by Γ, or gamma) at the antenna-to-tag interface. The symbol $|\triangle\Gamma|$ (delta gamma) represents the magnitude of the change in reflection coefficient from the non-modulating (absorptive) to the modulating (reflective) state.

3.2.1 Modulation as Related to $|\triangle\Gamma|$

Figure 3-1 illustrates the measured magnitude of the difference between the two states of the reflection coefficient:

$$|\Delta\Gamma| = |\Gamma_{\text{mod\_on}} - \Gamma_{\text{mod\_off}}|$$

When a tag is transmitting information to a reader, the tag modulator switches its reflection coefficient between the two states, producing modulated (information-bearing) sidebands in the reflected signal. The amount of energy in the modulated sidebands is directly proportional to $|\Delta\Gamma|^2$. As such, $|\Delta\Gamma|$ plays a key role in any RF link budget. It should be noted that resistance and other nonlinear parasitic effects in the modulator impose practical limits on the range of $|\Delta\Gamma|$. Note also that as the incident power level increases, the magnitude of the reflection coefficient in the modulator off state is intentionally increased, thereby reflecting excess incident power as CW to prevent damage to the tag's analog front end.

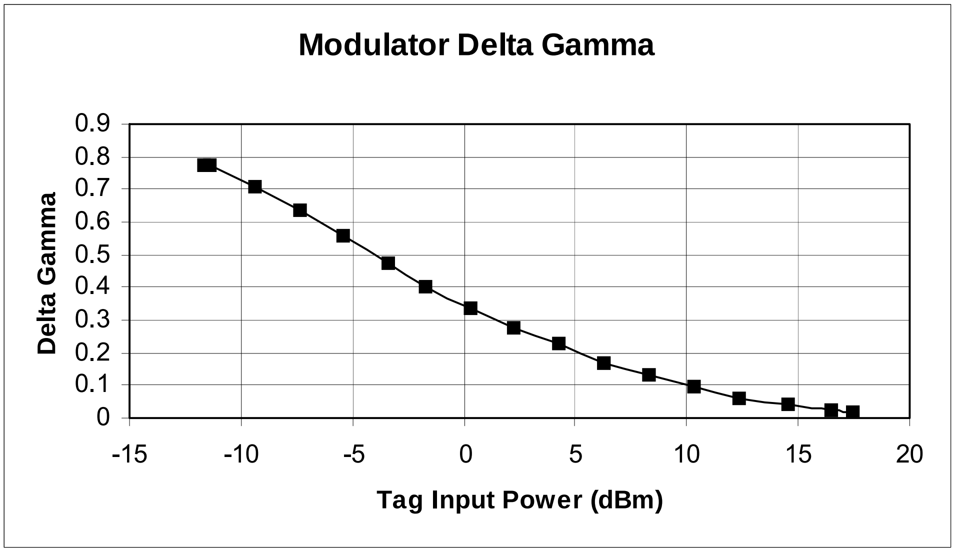


Figure 3-1 Measured Tag Delta-Gamma as a Function of Available Input Power

3.2.2 Radar Cross Section (RCS)

Tag RCS is the measure of the portion of the incident RF energy reflected isotropically back to a reader (a higher $|\triangle\Gamma|$ results in a larger RCS. But $|\triangle\Gamma|$ is not fixed; it changes with power). Figure 3-2 illustrates RCS as a function of $|\triangle\Gamma|$. RCS is given by:

$$\sigma_{bs} = \frac{P_{received}}{P_{incident}} \cdot 4\pi R^2$$

where σ_{bs} is the radar cross section; P_{incident} is the power incident on the tag, and P_{received} is the power at the antenna observing the tag's backscattered signal. Radar-cross section and $|\triangle\Gamma|$are related by:

$$\sigma_{bs} = \frac{\lambda^2}{4\pi} \cdot G_{Tag}^2 \cdot \left|\Delta\Gamma^2\right|$$

where G_{Tag} is the gain of the tag antenna.

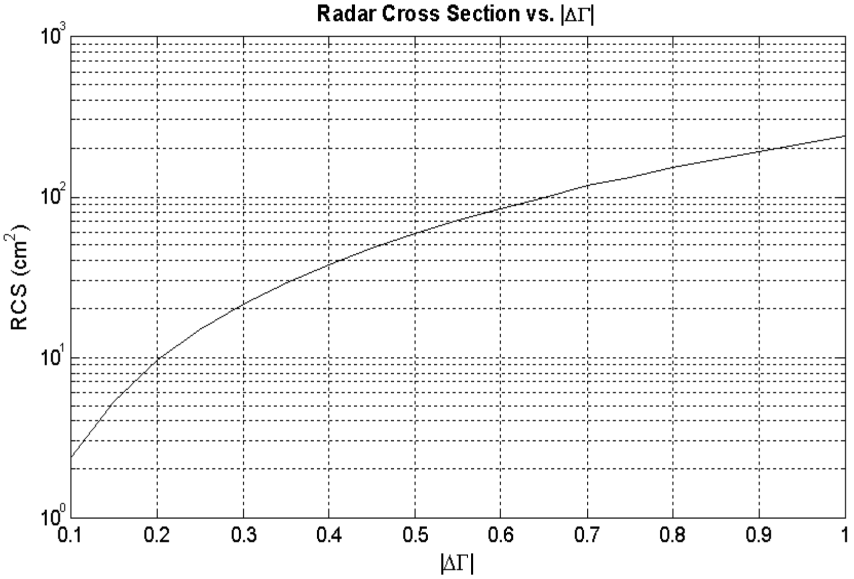


Figure 3-2 Tag radar cross section (RCS) as a function of |ΔΓ| (assumes half-wave dipole tag antenna and carrier frequency of 915 MHz)

If a tag is in close proximity to a reader, it will reflect a different amount of power than if the tag is at the limit of range. If the power level transmitted by the reader is known, and if the path loss to the tag is known, then one can determine |△Γ|. At lower power levels (long range), a large |△Γ|is desired, as this increases the tag's RCS, and hence its read/write range. But at higher power levels, a lower level of reflection is preferred. As can be seen in Figure 3-1, as input power increases, |△Γ| decreases.

3.2.3 Reflection Coefficient as Function of Antenna Impedance

Complex backscatter strength

Figure 3-3 shows delta gamma at minimum sensitivity as a function of antenna impedance (showing change in backscatter strength as the antenna impedance is varied). Complex delta gamma relates to the power that a coherent receiver such as a reader would detect. The data shown is the aggregate of measured impedance and calculations. The contours show the magnitude of the change in reflection coefficient at the antenna/chip interface for modulating (backscattering) versus non-modulating (power absorbing) states. The polar plot field is the s_{11} of the tag antenna as measured from a 50 ohm system. The black-filled circle shows tag antenna design target.

$$|\Delta\Gamma| = |\Gamma_{\text{mod\_on}} - \Gamma_{\text{mod\_off}}|$$

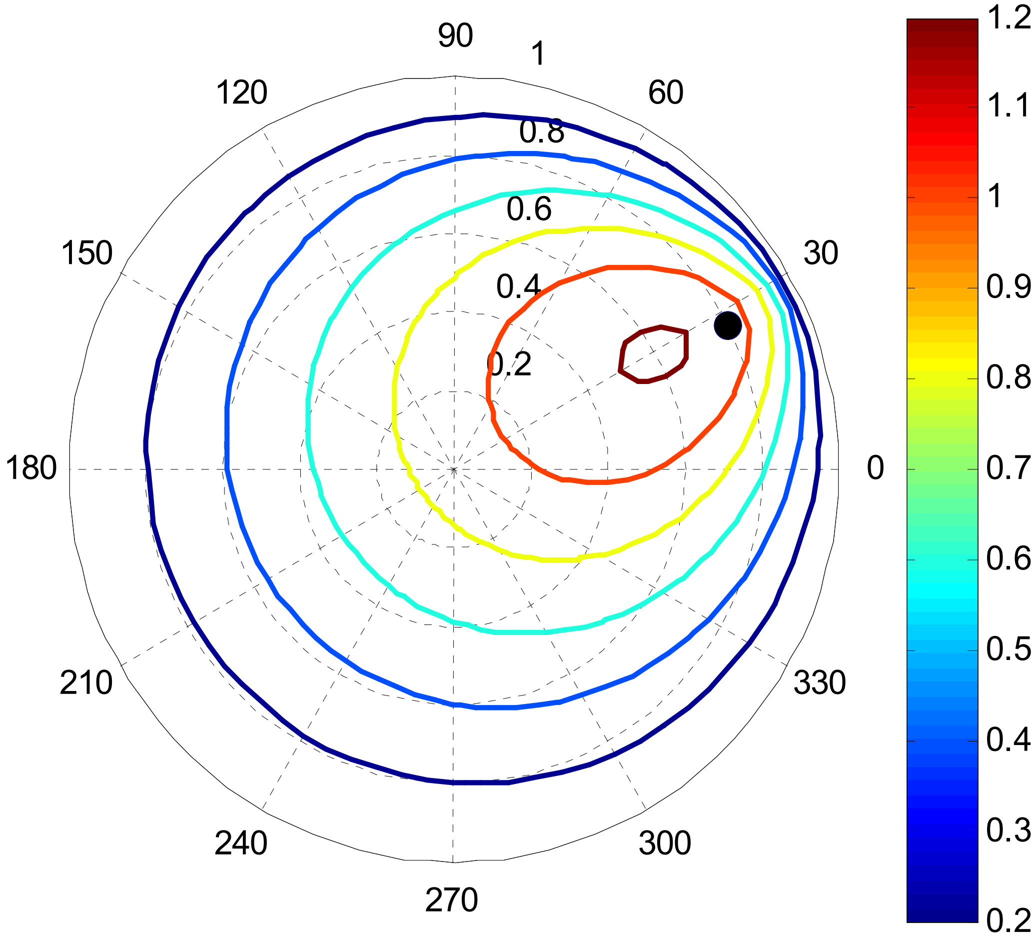


Figure 3-3 Tag reflection coefficient vs antenna impedance (total backscatter, magnitude of delta gamma)

Amplitude-modulated component of backscatter

The contours of Figure 3-4 show the change in reflection coefficient magnitudes at the antenna/chip interface for modulating (backscattering) versus non-modulating (power absorbing) states. The AM component of the backscatter relates to the power that monitoring or test equipment and other noncoherent receivers would detect. The polar plot field is the s_{11} of the tag antenna as measured from 50 ohm system. The black-filled circle shows tag antenna design target.

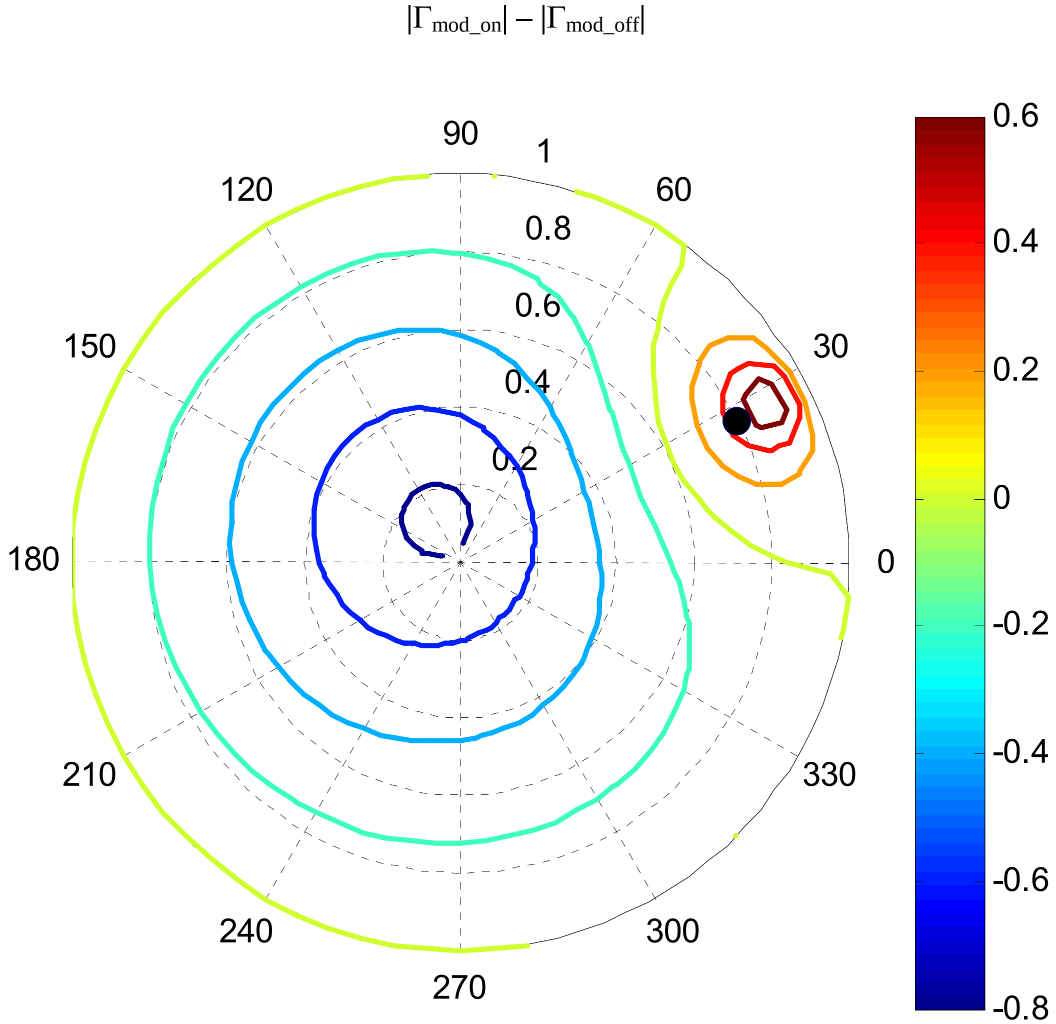


Figure 3-4 Amplitude-modulated component of backscatter

3.3 Making Connections

Impinj's patented rectifier technology (see 2.4, Power Management) is realized without the use of diodes. However, the bridge rectifier models shown in this section serve to illustrate the operating concepts, which are similar. The addition of a ground contact to this structure allows for three distinct antenna connection configurations, as follows:

- Single-ended
- Differential
- Shunt

Note that all three connection configurations use the same Monza/ID tag silicon; there is no change to the chip, itself. These possibilities enable a tremendous amount of flexibility for the antenna designer to tailor a tag to a specific market application. For each of these configurations, Impinj recommends a target source impedance for best operation (seesection 3.4). Details of the various configurations are described in the sections that follow.

3.3.1 Single-ended Connection

In this configuration, the signal is applied between one of the Monza/ID antenna ports and ground. The single-ended connection is the generally recommended configuration, as it exhibits the most efficient operation (highest sensitivity) of the three possible configurations.

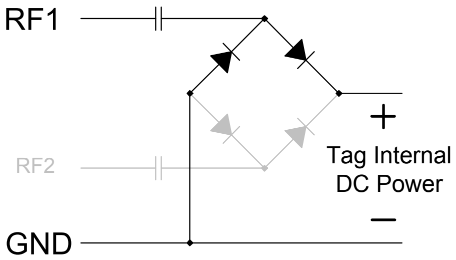


Figure 3-5 Rectifier model, single-ended configuration

The equivalent rectifier circuit for the single-ended configuration is shown in Figure 3-5, above (the portion of the circuit rendered in light gray is not electrically connected). Figure 3-6 shows an example of an antenna (Impinj Satellite™) designed for connection in this fashion.

Figure 3-6 Antenna designed for single-ended connection. Satellite antenna shown (L), with antenna trace connection detail (R). Note the diagonal pad contacts between RF1 and GND.

The single-ended configuration allows for a variety of possible chip/antenna connections, as shown in Figure 3-7, where the pads filled in black are those that are connected to the antenna traces. The dashed gray lines represent the electrical connections within the chip.

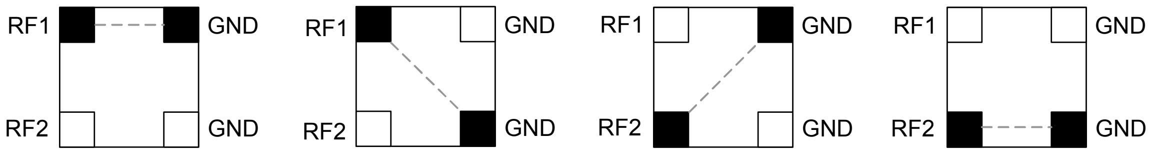


Figure 3-7 Chip/antenna connection possibilities for single-ended configuration

Note that Monza/ID features two electrically isolated antenna ports. As such, a second antenna can be connected in the same single-ended manner, allowing, for example, the use of a dual dipole design, which provides for antenna diversity that enables greater orientation flexibility. The use of Monza/ID's dual antenna inputs also captures more radiated energy, which extends tag read/write range.

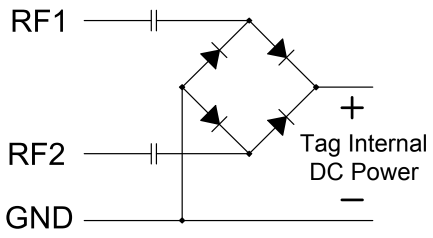


Figure 3-8 Rectifier model, dual single-ended configuration (e.g., dual dipole)

Figure 3-9 Two single-ended connections established for dual dipole antenna. Impinj Jumping Jack™ shown (L) with antenna trace detail (C) and corresponding chip/antenna connections (R).

3.3.2 Differential Connection

In this configuration, the signal is applied across the two antenna ports, with both ground pads left floating.

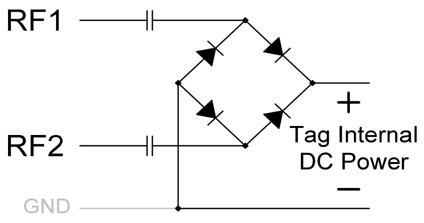


Figure 3-10 Rectifier model, differential configuration

Note that while both RF ports are connected in this configuration, it is intended for a single (dipole or loop) antenna. This arrangement represents a conventional application of a bridge rectifier, with RF1 connected to RF2 (see Figure 3-10). However, the parasitic capacitance that would normally appear from RF1-to-GND and RF2-to-GND has substantially less effect in the differential configuration (RF1-to-RF2). The lower effective capacitance and higher impedance benefits antennas with higher resistivity, e.g., those manufactured using conductive ink processes; the smaller value of inductive susceptance enables a larger loop, which yields a more efficient antenna (see Figure 3-11).

Figure 3-11 Antenna designed for differential connection. Impinj Disc™ shown (L) with antenna trace detail (C) and corresponding chip/antenna connections (R)

3.3.3 Shunt Connection

In this configuration, the two RF ports are shorted together (see Figure 3-12).

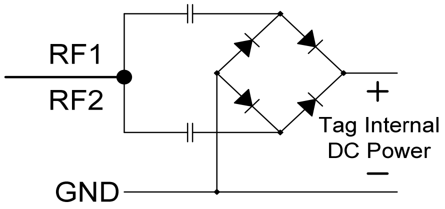


Figure 3-12 Rectifier model, shunt configuration

This scheme results in increased capacitance and greater sensitivity to low voltages, which benefits small loop and slot antennas (see Figure 3-13).

Figure 3-13 Small loop antenna (9 mm) designed for shunt connection. Impinj Button™ shown (L) with antenna trace detail (C) and corresponding chip/antenna connections (R)

3.4 Source Impedance

Table 3-2 shows the recommended antenna source impedances for Monza/ID tag silicon across center frequencies of the primary regions of operation (North America, Europe, and Japan) for the three connection configurations.

Figure 3-14 shows the same data graphically, with –1 dB sensitivity loss contour for the single-ended configuration. While the Smith chart plots only the case of F_c = 915 MHz, the results of the other frequencies fall within the resolution of the recommended point shown (indicated by the triangle inside the contour boundary; for the other frequencies considered, there is negligible change in the size and shape of the contour, although there is a slight phase shift). Note that due to the nonlinear nature of the tag circuits, this antenna source impedance is *not* the complex conjugate of the tag input impedance. The recommended source impedance values were determined empirically. Note that the suggested antenna impedance design target is near the *center* of the contour. The resulting mismatch loss from the point of *maximum* power transfer will be negligible; more importantly, it will result in more robust tag performance overall. Note also that a compromise value can be chosen to cover all worldwide frequencies.

Table 3-2 Recommended Antenna Source Impedances

Configuration		Single-ended	Differential	Shunt
Read Power Sensitivity		–11.5 dBm	–10.2 dBm	–10.5 dBm
Voltage Sensitivity		190mV$_{RMS}$	320mV$_{RMS}$	180mV$_{RMS}$
Linearized Model of Tag + Mounting Capacitance		530 Ω || 980fF	1050 Ω || 680fF	380 Ω || 1.87pF
Recommended Antenna Impedance at Minimum Sensitivity	**866 MHz** (Europe)	58 + j166 Ω	66 + j254 Ω	24 + j92 Ω
	915 MHz (North America)	52 + j158 Ω	59 + j242 Ω	21 + j88 Ω
	956 MHz (Japan)	48 + j153 Ω	55 + j233 Ω	20 + j84 Ω

Notes to table:

1. The recommended values shown are typical. Adhesives used for mounting the chip to the antenna add capacitance beyond Monza/ID's intrinsic capacitance (820 fF). Additional capacitance depends on adhesive properties and mounting parameters (values typically fall in the range of 150 fF to 250 fF).
2. Measurements reported herein were taken on mounted chips. As such, mounting capacitance is comprehended in these values.
3. Recommended source impedances were determined by load pull method.
4. Linearized tag model is the conjugate of the recommended source impedance, NOT the actual tag input impedance. This model is useful for calculating antenna mismatch.

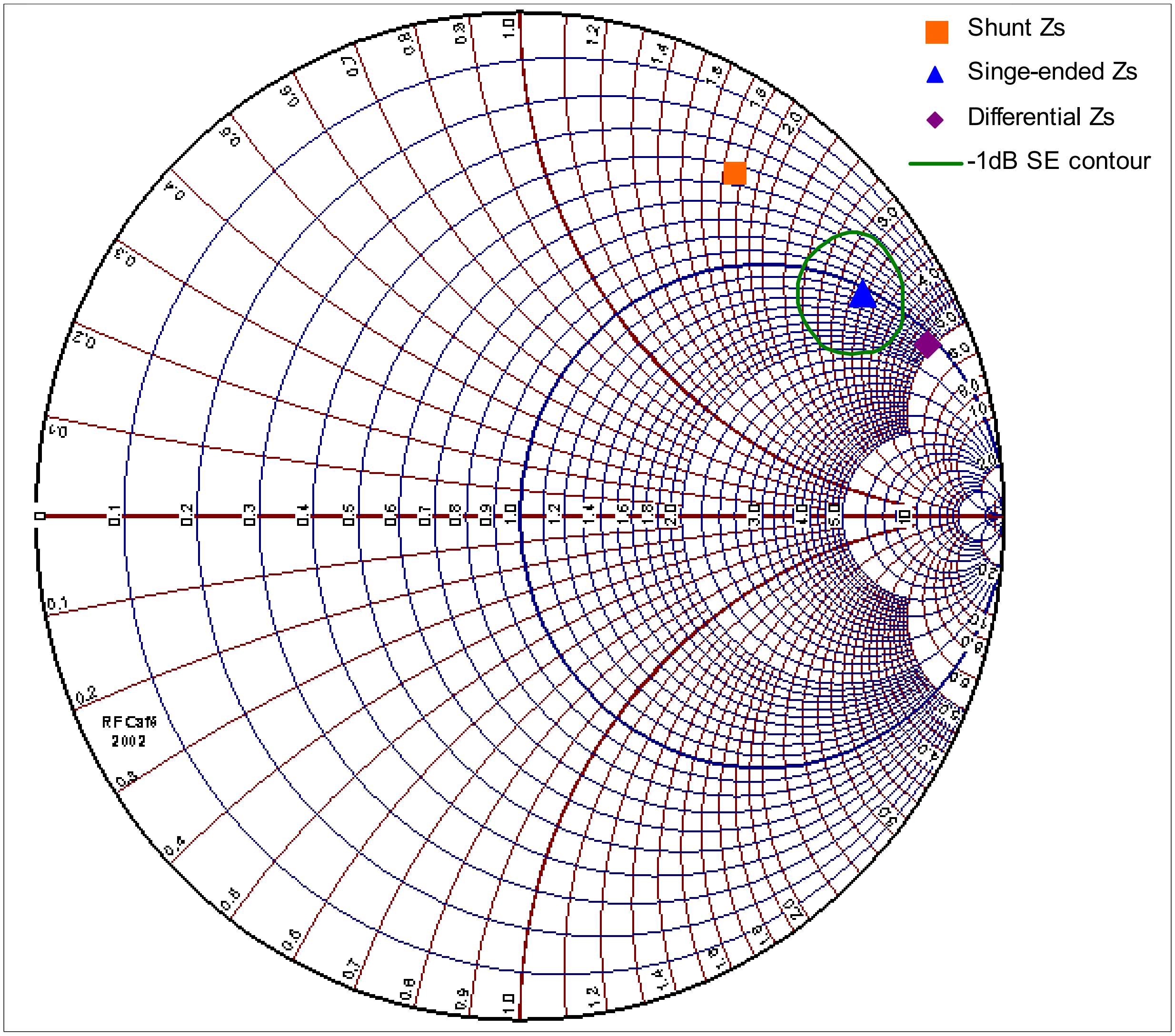


Figure 3-14 Recommended antenna source impedances for connection scenarios at 915 MHz

3.5 Reverse Link Signal Characteristics

Table 3-3 Reverse Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient $|\Delta\Gamma|$ due to Modulation		0.8			$|\Delta\Gamma| = |\Gamma_{reflect} - \Gamma_{absorb}|$ (per read/write sensitivity, Table 3-1)
Duty Cycle	45	50	55	%	
Symbol Period[1]	1.5625		25	µs	Baseband FM0
	3.125		200	µs	Miller-modulated subcarrier
Miller Subcarrier Frequency[1]	40		640	kHz	

Note 1. Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to arrive at absolute durations and frequencies.

4 Tag Memory

4.1 Memory Map

Figure 4-1depicts both a physical and logical chip memory map. The memory comprises Reserved, EPC, TID (which is ROM-based, and not user-writable), and factory-programmed UID (the serial ID, which occupies the Gen 2 User Memory space) memory banks.

MEM BANK #	MEM BANK NAME	MEM BANK BIT ADDRESS	BIT NUMBER															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	UID (NVM)	30_h-$3F_h$	SERIAL NUMBER (FACTORY-PROGRAMMED/LOCKED)															
		20_h-$2F_h$	SERIAL NUMBER (FACTORY-PROGRAMMED/LOCKED)															
		10_h-$1F_h$	SERIAL NUMBER (FACTORY-PROGRAMMED/LOCKED)															
		00_h-$0F_h$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10_2	TID (ROM)	10_h-$1F_h$	0	0	0	1	MODEL NUMBER[1]											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
01_2	EPC (NVM)	70_h-$7F_h$	EPC[15:0]															
		60_h-$6F_h$	EPC[31:16]															
		50_h-$5F_h$	EPC[47:32]															
		40_h-$4F_h$	EPC[63:48]															
		30_h-$3F_h$	EPC[79:64]															
		20_h-$2F_h$	EPC[95:80]															
		10_h-$1F_h$	PROTOCOL-CONTROL BITS (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	60_h-$6F_h$	MONZA/ID VALIDATION KEY (MS 4 BITS)[2]															
		50_h-$5F_h$	RESERVED FOR FACTORY USE															
		40_h-$4F_h$	RESERVED FOR FACTORY USE															
		30_h-$3F_h$	ZERO-VALUED PASSWORD (READ/WRITE LOCKED)															
		20_h-$2F_h$	ZERO-VALUED PASSWORD (READ/WRITE LOCKED)															
		10_h-$1F_h$	ZERO-VALUED PASSWORD (READ/WRITE LOCKED)															
		00_h-$0F_h$	ZERO-VALUED PASSWORD (READ/WRITE LOCKED)															

Note 1. The LSB of the Monza/ID model number is “don’t care.”
Note 2. The most significant 4 bits of this row are the Monza/ID validation key; the remaining 12 bits are reserved for factory use.

Figure 4-1 Physical / Logical Memory Map

4.2 Logical vs. Physical Bit Identification

For purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address describes the addressing used to access the memory.

4.3 Memory Banks

Described in the following sections are the contents of the NVM and ROM memory, and the parameters for their associated bit settings.

4.3.1 Reserved Memory

Monza/ID acts as though it has zero-valued passwords that are permanently read/write locked; the user may not alter this status. Note that a tag will not execute a kill operation if its Kill Password is all zeroes.

4.3.2 Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data. The Impinj MDID (Manufacturer Identifier) is 000000000001 (shown in Figure 4-1 as the lighter gray-shaded bits across both TID memory rows). The Monza/ID model number is shown in as the darker gray-shaded bits in TID memory row10_h – $1F_h$. The non-shaded bit locations in TID row 00_h – $0F_h$ store the EPCglobal Class ID (0xE2).

4.3.3 EPC Memory

EPC memory contains the 16 protocol-control bits (PC) at memory addresses 10_h – $1F_h$, a CRC16 at memory addresses 00_h – $0F_h$, and an EPC value beginning at address 20_h. A reader accesses EPC memory by setting MemBank = 01_2 in the appropriate command, and providing a memory address using the extensible-bit-vector (EBV) format. The PC, CRC16, and EPC are stored MSB first (i.e., the EPC's MSB is stored in location 20_h).

The EPC written at time of manufacture is as follows:

Impinj Part Number	96-Bit EPC Value Preprogrammed at Manufacture (hex)
IPJ_W_I_(A or C)	3008 33b2 ddd9 0680 0000 0000

4.3.4 UID

This feature complies with ISO 15963, which specifies the numbering system of a permanent unique identifier (UID). Address range 10_h – $3F_h$ has been allocated to the factory-programmed serial number (48 bits). Note that the UID occupies the Gen 2 User Memory space.

5 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the tag. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Temperature

Several different temperature ranges will apply over unique operating and survival conditions. Table 5-1 lists the ranges that will be referred to in this specification. Tag functional and performance requirements are met over the operating range, unless otherwise specified.

Table 5-1 Temperature parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Extended Operating Temperature	–40		+65	°C	Default range for all functional and performance requirements
Storage Temperature[1]	–40		+85	°C	
Assembly Survival Temperature			+150	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

Note 1. This assumes wafer only. If UV film-mounted, storage temperature MUST NOT exceed 25 °C.

5.2 Input Damage Levels

The tag is guaranteed to survive the inputs specified in Table 5-2.

Table 5-2 ESD and input limits

Parameter	Minimum	Typical	Maximum	Units	Comments
ESD			2,000	V	HBM (Human Body Model)
Reader antenna power with tag sitting on antenna			36[1]	dBm	Tag has 10 cm half-wave dipole antenna
DC input voltage			± 3.5	volts	Applied across two pads
DC input current			± 0.5	mA	Into any input pad

Note 1. Assumes tag has half-wave dipole antenna. While maximum radiated reader power is +36 dBm for both Read and Write operations, the maximum power the tag should receive is +20 dBm (see Table 3-1).

5.3 NVM Use Model

Tag memory will endure 100k write cycles and 50-year retention.

6 Ordering Information

Part Number	Form	Product	Processing Flow
IPJ_W_I_A	Wafer	Monza/ID	Raw: non-bumped, non-thinned
IPJ_W_I_C	Wafer	Monza/ID	Bumped, thinned (to 6 mils, or ~150 μm), and sawn

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